

Appl. No. 10/714,075  
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Reply to Office Action of 11/15/2005

IN THE CLAIMS

Please amend claims 2, 7, 16, and 22 as follows below.

Please add new claim 40 as follows below.

The following listing of claims replaces all prior versions, and listings, of claims in the application:

MARKED UP VERSION OF CLAIMS

- 1           1.    (Cancelled)
  
- 1           2.    (Currently Amended) An integrated circuit to  
2           interface to memory, the integrated circuit comprising:  
3                a first off chip driver calibration terminal to  
4           couple to an external pull-up resistor;  
5                a first tristate driver having an output coupled  
6           to the first off chip driver calibration terminal for  
7           pull-up calibration of pull-up transistors;  
8                a second off chip driver calibration terminal to  
9           couple to an external pull-down resistor;  
10           a second tristate driver having an output coupled  
11           to the second off chip driver calibration terminal for  
12           pull-down calibration of pull-down transistors;

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13           a first switch coupled between the first off chip  
14       driver calibration terminal and a voltage reference  
15       node; and

16           a second switch coupled between the second off  
17       chip driver calibration terminal and the voltage  
18       reference node. [[:]]

19       ~~wherein the first switch and the second switch are~~  
20       ~~selectively closed to generate an internal voltage~~  
21       ~~reference on the voltage reference node with which an~~  
22       ~~input signal is compared in order to receive data.~~

1       3.    (Original)     The integrated circuit of claim 2,  
2       wherein

3           the first switch is selectively closed and the  
4       second switch is selectively opened to generate a pull-  
5       up calibration voltage on the voltage reference node to  
6       calibrate an off-chip driver.

1       4.    (Original)     The integrated circuit of claim 3,  
2       wherein

3           the first switch is selectively opened and the  
4       second switch is selectively closed to generate a pull-  
5       down calibration voltage on the voltage reference node  
6       to further calibrate the off-chip driver.

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1           5.     (Previously Presented)     An integrated circuit to  
2     interface to memory, the integrated circuit comprising:  
3           a first off chip driver calibration terminal to  
4     couple to an external pull-up resistor;  
5           a second off chip driver calibration terminal to  
6     couple to an external pull-down resistor;  
7           a first switch coupled between the first off chip  
8     driver calibration terminal and a voltage reference  
9     node;  
10          a second switch coupled between the second off  
11     chip driver calibration terminal and the voltage  
12     reference node; and  
13          a plurality of input receivers each having a first  
14     input coupled to the voltage reference node and a  
15     second input coupled to a respective data terminal of a  
16     plurality of data terminals.

1           6.     (Original)           The integrated circuit of claim 5,  
2     wherein  
3           each input receiver includes  
4           a comparator having a first input coupled to the  
5     voltage reference node and a second input coupled to  
6     the respective data terminal, the data terminal to  
7     couple to an off-chip output driver for calibration.

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1           7.    (Currently Amended) An integrated circuit to  
2           interface to memory, the integrated circuit comprising:  
3                a first off chip driver calibration terminal to  
4           couple to an external pull-up resistor;  
5                a first tristate driver having an output coupled  
6           to the first off chip driver calibration terminal for  
7           pull-up calibration of pull-up transistors;  
8                a second off chip driver calibration terminal to  
9           couple to an external pull-down resistor;  
10               a second tristate driver having an output coupled  
11           to the second off chip driver calibration terminal for  
12           pull-down calibration of pull-down transistors;  
13                a first switch coupled between the first off chip  
14           driver calibration terminal and a voltage reference  
15           node;  
16                a second switch coupled between the second off  
17           chip driver calibration terminal and the voltage  
18           reference node; and  
19                a switch controller having a mode input, a first  
20           control output coupled to a control input of the first  
21           switch, and a second control output coupled to a  
22           control input of the second switch, the switch  
23           controller to control the opening and closing of the  
24           first switch and the second switch in response to the  
25           mode input.

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1           8.     (Previously Presented)     The integrated circuit of  
2     claim 7, wherein

3                 the first switch and the second switch are  
4     selectively closed to generate an internal voltage  
5     reference on the voltage reference node with which an  
6     input signal is compared in order to receive data;

7                 the first switch is selectively closed and the  
8     second switch is selectively opened to generate a pull-  
9     up calibration voltage on the voltage reference node to  
10    calibrate an off-chip driver; and

11                the first switch is selectively opened and the  
12    second switch is selectively closed to generate a pull-  
13    down calibration voltage on the voltage reference node  
14    to further calibrate the off-chip driver.

1           9.     (Previously Presented)     The integrated circuit of  
2     claim 2, wherein

3                 the integrated circuit is a memory controller.

1           10.    (Previously Presented)     The integrated circuit of  
2     claim 2, wherein

3                 the integrated circuit is a processor.

1           11.    (Original)           A method in an integrated circuit  
2     for interfacing to a memory, the method comprising:

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3           if in an off-chip driver calibration mode for a  
4           pull-up, then  
5                selecting a pull-up calibration terminal to  
6           be coupled to a voltage reference node to provide  
7           a pull-up calibration voltage thereon, and  
8                calibrating a pull-up of an off chip driver;  
9           if in an off-chip driver calibration mode for a  
10          pull-down, then  
11                selecting a pull-down calibration terminal to  
12          be coupled to the voltage reference node to  
13          provide a pull-down calibration voltage thereon,  
14          and  
15                calibrating a pull-down of the off chip  
16          driver;  
17          and,  
18          if in a normal mode to receive data, then  
19                selecting the pull-up calibration terminal  
20          and the pull-down calibration terminal to be  
21          coupled to the voltage reference node to provide a  
22          reference voltage thereon, and  
23                receiving data from a data terminal.

1          12. (Original)       The method of claim 11 further  
2          comprising:  
3                prior to selecting, calibrating and receiving,

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4                    coupling an external pull-up resistor to the  
5                    pull-up calibration terminal; and  
6                    coupling an external pull-down resistor to  
7                    the pull-down calibration terminal.

1           13. (Original)        The method of claim 11, wherein  
2           the receiving data from the data terminal includes  
3           comparing the reference voltage on the voltage  
4           reference node with an incoming signal on the data  
5           terminal.

1           14. (Original)        The method of claim 13, wherein  
2           the calibrating of the pull-up of the off chip  
3           driver includes  
4           comparing the pull-up calibration voltage on the  
5           voltage reference node with an incoming signal on the  
6           data terminal.

1           15. (Original)        The method of claim 14, wherein  
2           the calibrating of the pull-down of the off chip  
3           driver includes  
4           comparing the pull-down calibration voltage on the  
5           voltage reference node with an incoming signal on the  
6           data terminal.

1           16. (Currently Amended)    A system comprising:

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2           a processor for executing instructions and  
3       processing data;  
4           a double data rate memory device to store data  
5       from the processor and to read data to the processor;  
6           an external pull-up resistor having a first end  
7       coupled to a first power supply terminal;  
8           an external pull-down resistor having a first end  
9       coupled to a second power supply terminal; and  
10          a memory controller coupled between the double  
11       data rate memory device and the processor, the memory  
12       controller including  
13           a pull-up calibration terminal coupled to a  
14       second end of the external pull-up resistor,  
15           a first tristate driver having an output  
16       coupled to the pull-up calibration terminal for  
17       pull-up calibration of pull-up transistors in the  
18       double data rate memory device,  
19           a pull-down calibration terminal coupled to a  
20       second end of the external pull-down resistor,  
21           a second tristate driver having an output  
22       coupled to the pull-down calibration terminal for  
23       pull-down calibration of pull-down transistors in  
24       the double data rate memory device,  
25           a voltage reference node,  
26           a first switch having a first switch  
27       connection coupled to the pull-up calibration



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28 terminal and a second switch connection coupled to  
29 the voltage reference node, and  
30 a second switch having a first switch  
31 connection coupled to the pull-down calibration  
32 terminal and a second switch connection coupled to  
33 the voltage reference node.

1 17. (Original) The system of claim 16, wherein  
2 the memory controller is an integrated circuit  
3 separate from the processor.

1 18. (Original) The system of claim 16, wherein  
2 the processor is an integrated circuit and  
3 includes the memory controller.

1 19. (Original) The system of claim 16, wherein  
2 the memory controller further includes  
3 a switch controller having a mode input, a  
4 first control output coupled to a control input of  
5 the first switch, and a second control output  
6 coupled to a control input of the second switch,  
7 the switch controller to control the opening and  
8 closing of the first switch and the second switch  
9 in response to the mode input.

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1           20. (Previously Presented)    The system of claim 19,  
2           wherein  
3                 the first switch and the second switch are  
4           selectively closed to generate an internal voltage  
5           reference on the voltage reference node with which an  
6           input signal is compared in order to receive data;  
7                 the first switch is selectively closed and the  
8           second switch is selectively opened to generate a pull-  
9           up calibration voltage on the voltage reference node to  
10          calibrate a driver of the DDR memory device; and  
11                 the first switch is selectively opened and the  
12          second switch is selectively closed to generate a pull-  
13          down calibration voltage on the voltage reference node  
14          to further calibrate the driver of the DDR memory  
15          device.

1           21. (Cancelled)

1           22. (Currently Amended)    A processor for a computer  
2           system, the processor including:  
3                 a memory controller to interface to memory, the  
4           memory controller having  
5                 a pull-up calibration terminal to couple to  
6           an external pull-up resistor,

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7                    a first tristate driver having an output  
8                    coupled to the pull-up calibration terminal for  
9                    pull-up calibration of pull-up transistors in the  
10                   double data rate memory device,  
11                   a pull-down calibration terminal to couple to  
12                   an external pull-down resistor,  
13                   a second tristate driver having an output  
14                   coupled to the pull-down calibration terminal for  
15                   pull-down calibration of pull-down transistors in  
16                   the double data rate memory device,  
17                   a voltage reference node,  
18                   a first switch coupled between the pull-up  
19                   calibration terminal and the voltage reference  
20                   node,  
21                   a second switch coupled between the pull-down  
22                   calibration terminal and the voltage reference  
23                   node, and  
24                   a switch controller having a mode input, a  
25                   first control output coupled to a control input of  
26                   the first switch, and a second control output  
27                   coupled to a control input of the second switch,  
28                   the switch controller to control the opening and  
29                   closing of the first switch and the second switch  
30                   in response to the mode input.

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1           23. (Previously Presented)    The processor of claim  
2           22, wherein  
3               the first switch and the second switch are  
4           selectively closed to generate an internal voltage  
5           reference on the voltage reference node with which an  
6           input signal is compared in order to receive data from  
7           a driver of a memory device;  
8               the first switch is selectively closed and the  
9           second switch is selectively opened to generate a pull-  
10          up calibration voltage on the voltage reference node to  
11          calibrate the driver of the memory device; and  
12          the first switch is selectively opened and the  
13          second switch is selectively closed to generate a pull-  
14          down calibration voltage on the voltage reference node  
15          to further calibrate the driver of the memory device.

1           24. (Original)           A packaged integrated circuit to  
2           interface to memory, the packaged integrated circuit  
3           comprising:  
4               a first off-chip driver calibration terminal to  
5           couple to a first external resistor;  
6               a second off-chip driver calibration terminal to  
7           couple to a second external resistor;  
8               a first plurality of field effect transistors  
9           having sources coupled in parallel together to the

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10 first off-chip driver calibration terminal and drains  
11 coupled in parallel together to a voltage reference  
12 node; and  
13 a second plurality of field effect transistors  
14 having drains coupled in parallel together to the  
15 second off-chip driver calibration terminal and sources  
16 coupled in parallel together to the voltage reference  
17 node.

1 25. (Original) The packaged integrated circuit of  
2 claim 24 wherein  
3 the first plurality of field effect transistors  
4 and the second plurality of field effect transistors  
5 are p-channel field effect transistors.

1 26. (Original) The packaged integrated circuit of  
2 claim 24 wherein  
3 the first plurality of field effect transistors  
4 and the second plurality of field effect transistors  
5 are n-channel field effect transistors.

1 27. (Original) The packaged integrated circuit of  
2 claim 24 wherein  
3 the first plurality of field effect transistors  
4 are p-channel field effect transistors, and

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5           the second plurality of field effect transistors  
6           are n-channel field effect transistors.

1           28. (Original)       The packaged integrated circuit of  
2           claim 24 wherein

3           the first plurality of field effect transistors  
4           are n-channel field effect transistors, and  
5           the second plurality of field effect transistors  
6           are p-channel field effect transistors.

1           29. (Original)       The packaged integrated circuit of  
2           claim 24 wherein

3           the first plurality of field effect transistors  
4           are p-channel field effect transistors and n-channel  
5           field effect transistors having sources coupled in  
6           parallel together and drains coupled in parallel  
7           together, and

8           the second plurality of field effect transistors  
9           are p-channel field effect transistors and n-channel  
10          field effect transistors having sources coupled in  
11          parallel together and drains coupled in parallel  
12          together.

1           30. (Original)       The packaged integrated circuit of  
2           claim 24 further comprising:

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3           a switch controller having a mode input, a first  
4           plurality of switch control signals coupled to  
5           respective gates of the first plurality of field effect  
6           transistors, a second plurality of switch control  
7           signals coupled to respective gates of the second  
8           plurality of field effect transistors, the switch  
9           controller to control the switching of the first and  
10          second plurality of field effect transistors.

1          31. (Original)       The packaged integrated circuit of  
2          claim 24 further comprising:

3           a plurality of input receivers each having a first  
4           input coupled to the voltage reference node and a  
5           second input coupled to respective data terminals to  
6           receive data.

1          32. (Original)       The packaged integrated circuit of  
2          claim 31, wherein

3           each input receiver includes  
4           a comparator having a first input coupled to the  
5           voltage reference node and a second input coupled to a  
6           respective data terminal to calibrate a pull-up and a  
7           pull-down of an off-chip output driver.

1          33. (Original)       The packaged integrated circuit of  
2          claim 32, wherein

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3           the comparator of each input receiver further to  
4           receive data by comparing a reference voltage on the  
5           reference node with an input signal on the respective  
6           data terminal.

1           34. (Previously Presented) The integrated circuit of  
2           claim 5, further comprising:

3           a switch controller having a mode input, a first  
4           control output coupled to a control input of the first  
5           switch, and a second control output coupled to a  
6           control input of the second switch, the switch  
7           controller to control the opening and closing of the  
8           first switch and the second switch in response to the  
9           mode input.

1           35. (Previously Presented) The integrated circuit of  
2           claim 34, wherein

3           the first switch and the second switch are  
4           selectively closed to generate an internal voltage  
5           reference on the voltage reference node with which an  
6           input signal is compared in order to receive data;

7           the first switch is selectively closed and the  
8           second switch is selectively opened to generate a pull-  
9           up calibration voltage on the voltage reference node to  
10          calibrate an off-chip driver; and



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11           the first switch is selectively opened and the  
12           second switch is selectively closed to generate a pull-  
13           down calibration voltage on the voltage reference node  
14           to further calibrate the off-chip driver.

1           36. (Previously Presented) The integrated circuit of  
2           claim 7, wherein  
3           the first switch and the second switch are  
4           selectively closed to generate an internal voltage  
5           reference on the voltage reference node with which an  
6           input signal is compared in order to receive data.

1           37. (Previously Presented) The integrated circuit of  
2           claim 7, wherein  
3           the first switch is selectively closed and the  
4           second switch is selectively opened to generate a pull-  
5           up calibration voltage on the voltage reference node to  
6           calibrate an off-chip driver.

7           38. (Previously Presented) The integrated circuit of  
8           claim 7, wherein  
9           the first switch is selectively opened and the  
10          second switch is selectively closed to generate a pull-  
11          down calibration voltage on the voltage reference node  
12          to calibrate an off-chip driver.

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13           39. (Previously Presented)   The processor of claim  
14           23, wherein  
15           the memory device is a double data rate (DDR)  
16           memory device.

1           40. (New)           The integrated circuit of claim 2,  
2           wherein  
3           the first switch and the second switch are  
4           selectively closed to generate an internal voltage  
5           reference on the voltage reference node with which an  
6           input signal is compared in order to receive data.

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